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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,525	03/08/2002	Keishiro Okamoto	020214	3829

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/092,525	OKAMOTO ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/19/2006 has been entered. An action on the RCE follows.

2. The amendment filed on 3/28/2006 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-6, 8-10 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty, US patent No. 6,611,419 in view of Gnadinger, US patent No. 5,229,647.

Regarding claim 1, Chakravorty teaches (figs. 2 and 3) a semiconductor apparatus, comprising: a support substrate (310) having straight through holes filled with conductor (323, through holes 323 within portion of the substrate 310) in conformity

with a first uniform pitch, capacitors (330) formed on the support substrate (310) comprising a lower electrode (329) having a first wide area (region where lower electrode is formed) and a first cut-away portion (refer to fig. 3, the cut-away portions are the regions where the through holes go through), a dielectric film (340) covering the first wide area (refer to fig. 3) and an upper electrode (326) having a second wide area (region where 326 is formed) and a second cut-away portion (region where through hole 323 goes through adjacent the capacitor region) the first and second wide areas facing via the dielectric film (340) to establish a capacitance (330), wiring layer (322) formed on the support substrate, leading some of the through holes filled with conductor upwards via the capacitor (330), having branches (322 branches out of 323), above the upper electrode (326) to form wires (321) of second uniform pitch narrower than the first uniform pitch (the pitch for 321 appears to be narrower than 323, also refer to col. 4, lines 42-51) and plural semiconductor elements (IC die 300) disposed on the wiring layer (321), having terminals (the IC die inherently has terminals) in conformity with the second uniform pitch, and connected with the wiring layer (322) via the terminals (refer to fig. 3).

Chakravorty does not teach a support substrate made of a semiconductor substrate. However Chakravorty teaches (col. 4, lines 23-25) that die (200/300) and substrate (210/310) can be of any type.

Gnadinger teaches (fig. 4, col. 3, lines 37-57) the use of a semiconductor wafer (10) as a support in the structure of forming an interconnect structure.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the semiconductor substrate taught by Gnadinger in the structure of Chakravorty in order to form a high density interconnection structure.

Regarding claim 2, Chakravorty teaches substantially the entire claimed structure of claim 1 above including a circuit board (320, col. 4, lines 59-67) having wiring of a first uniform pitch and connected to lower surfaces of the through holes (323) filled with conductor.

Regarding claims 4 and 5, Chakravorty teaches (fig. 3) substantially the entire claimed structure of claim 1 above including the support substrate is a Si substrate (10) having through holes (refer to fig. 3 of Gnadinger) with an insulation film (24) formed on the side walls of the holes, and the through holes filled with conductor are metallic conductors packed in the through holes.

Regarding claim 6, Chakravorty teaches substantially (figs. 4 of Gnadinger, col. 3, lines 37-57) the entire claimed structure of claim 1 above including the insulation film is a silicon oxide film (24) and lower surfaces of the silicon substrate are also covered with an insulating material (27).

The limitation that the silicon oxide film is formed by thermal oxidation is not given patentable weight because, this is considered a product-by-process claim. "[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is

unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claims 8 and 9, Chakravorty teaches substantially the entire claimed structure of claim 1 above including the through holes filled with conductor (fig. 3, 323) include a first signal wire; the wiring layer (322) contains a second signal wire (321 also serves as a signal via) for leading the first signal wire substantially vertically (fig. 3); and the capacitor has electrodes (326 and 329) with a vacancy (region between the electrodes) around a region where the second signal wire is located.

Regarding claim 10, Chakravorty teaches (fig. 3) substantially the entire claimed structure of claim 1 above except explicitly stating that the insulation layer disposed on the support substrate, have a thermal expansion coefficient of 10 ppm/°C or less in the in-plane direction, and insulates the wiring layer and the capacitor.

Parameters such as coefficient of thermal expansion and heat capacity in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thermal expansion coefficient of Chakravorty structure as claimed in order to improve the thermal property of the device.

Regarding claim 13, Chakravorty teaches (fig. 3) substantially the entire claimed structure of claim 1 above including the wiring layer (322) contains a wiring connecting the plural semiconductor elements with each other (die 300 appears to be connected to each other).

Regarding claim 14, Chakravorty teaches (fig. 3) substantially the entire claimed structure of claim 1 above including another circuit part (320) connected with the wiring layer (322) via (331).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty, Gnadinger and in view of Kabumoto et al., US patent No. 5,883,428.

Regarding claim 7, Chakravorty teaches (fig. 1) substantially the entire claimed structure of claim 1 above except explicitly teaching that the capacitor is a decoupling capacitor connected between power wires.

Decoupling capacitors are conventional in the art and are also taught by Kabumoto (fig. 1) for reducing power-supply noise (col. 5, lines 23-48).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the decoupling capacitors taught by Kabumoto in the structure of Chakravorty in order to reduce noise between the power wires of Chakravorty's integrated device.

6. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty, Gnadinger and in view of Cuchiaro et al. US patent No. 5,888,585.

Regarding claims 11 and 12, Chakravorty teaches substantially the entire claimed structure of claim 1 above except explicitly stating that the capacitor has a capacitor dielectric layer made of an oxide containing at least one of Ba, Sr and Ti, and

a pair of capacitor electrodes sandwiching the capacitor dielectric layer and containing at least partially one of Pt, Ir, Ru, Pd or any of their oxides.

Cuchiaro teaches a charge storage device including high dielectric material comprising barium and platinum electrode in the process of making an integrated device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the capacitor structure of Chakravorty device using the materials taught by Cuchiaro in order to form a capacitor structure that is smaller in size and with less leakage current.

Response to Arguments

7. Applicant's arguments filed 3/18/2006 have been fully considered but they are not persuasive. Applicant argues that Chakravorty does not teach straight through holes and there is no uniformity in the pitch below or above the capacitor. Applicant further argues a person of ordinary skill in the art would not be motivated to combine Gnadinger in the structure of Chakravorty, because the manufacturing processes of a ceramic substrate and a semiconductor substrate are completely different.

Figure 3 of Chakravorty teaches straight through holes (323) that are straight within the support substrate (310). Furthermore the through holes with conductors (323) appear to have a uniform pitch. With regards to applicant's argument that it would not be obvious to replace the substrate of Chakravorty with Gnadinger, as stated in the rejection above, Chakravorty teaches that the substrate of fig. 2 (col. 4, lines 23-25) that

die (200/300) and substrate (210/310) can be of any type. This implies that the substrate can be a semiconductor substrate such as silicon that is commonly used in the art of semiconductor devices. Furthermore Gnadinger teaches a silicon substrate with interconnections/wiring formed in it. Therefore it is within the skill of ordinary person in the art to try and replace the substrate of Chakravorty with the substrate of Gnadinger in order to improve the packing density of the device.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571)-272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SAG
May 30, 2006

Douglas W. Owens 5/30/06

DOUGLAS W. OWENS
PRIMARY EXAMINER